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Sub-cooled SFCL Device and Modules for Power Transmission / Distribution

Juan-Carlos H. Llambes, Ph.D.
SFCL Program Manager / Senior High Voltage Engineer

University of Houston: V. Selvamanickam, I. Kesgin, G. Majkic.

CAPS, Florida State University: J. Langston, M. Steurer, F. Bogdan, J. Hauer, D. Crook, S. Ranner, T. Williams, M. Coleman.

SuperPower: D. Hazelton, J. Duval, M. Albertini, S. Repnoy.

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celebrating 10 years 2000 ~ 2010

- Program Outline & Objectives
- Accomplishments & Results
- Planned Performance & Milestones
- Summary

Previous 2009 program focused on module development

- The current project purpose is focused on the development of second-generation (2G) high-temperature superconductor (HTS) based modules for a superconducting fault current limiter (SFCL) for operation at voltage levels up to transmission level. These modules can then be used in later proof-of-concept and alpha/beta prototypes.

- Primary objectives for FY09:
  - continue to improve our understanding of the impact of recovery under load (RUL) on the module design
  - continue to optimize the performance of the 2G HTS wire
  - investigate the performance of more compact alternate ‘module’ concepts
  - test FCL module components at rated voltage in a cryogenic environment

2010 Program focused on sub-cooled / pressurized SFCL device and module development

- The current project purpose is focused on the Sub-cooled / Pressurized development of 2G HTS-based modules for a SFCL for operation at voltage levels up to transmission level.

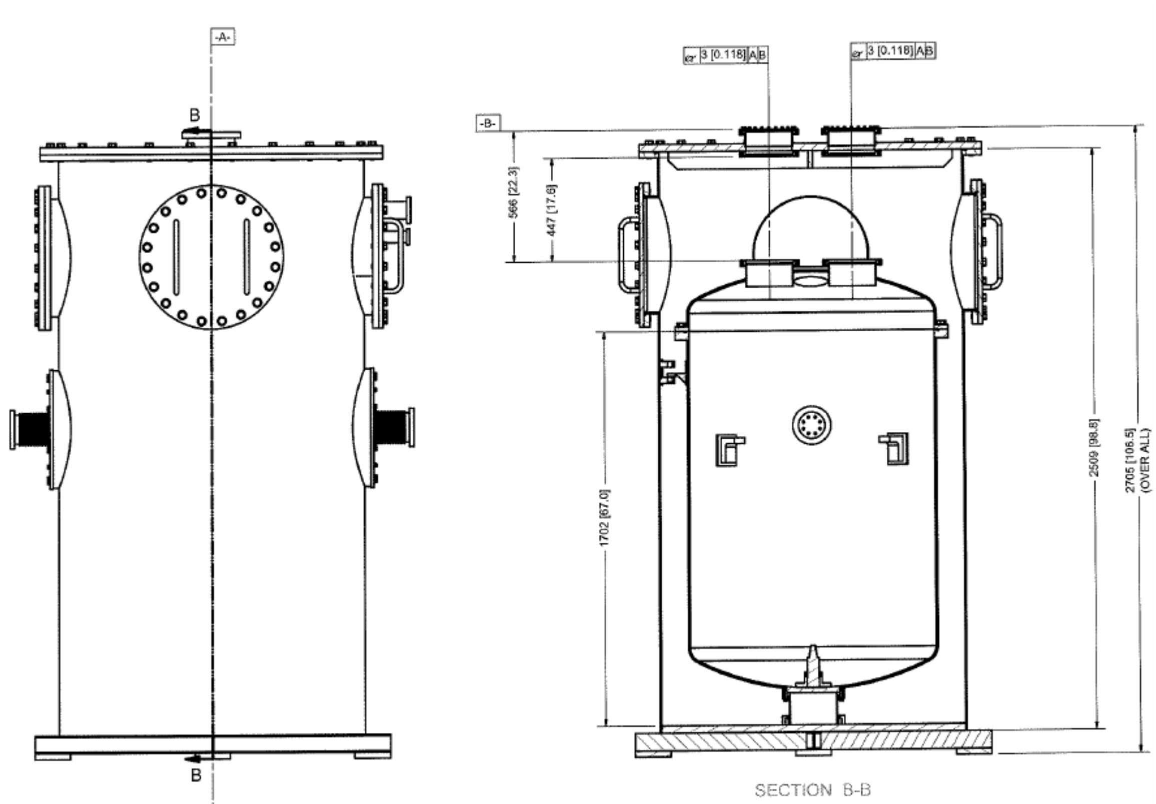
- Primary objectives for 2010:
  - continue improving our understanding Fault Current Limitation with and without recovery under load (RUL) on the module design in LN2 sub-cooled / pressurized conditions
  - continue optimizing the performance of the 2G HTS wire
  - investigate performance of more compact alternate ‘module’ concepts
  - test FCL module components at rated voltage in a cryogenic environment
  - study 2G HTS Superconductor Voltage and Resistance limitation in open bath versus sub-cooled conditions.
  - study and understanding of frequency dependence on SFCL device and modules

Modular SFCL system design – components integration

Modular SFCL device design specifications

- **2G tape** – Jc, J/cm/tape, RUL Arms/tape, mechanical, thermal and electrical properties
- **Shunt Coils** – Zsh = Rsh + jXsh, X/R ratio, EM force withstand, thermal and electrical properties, connectors, size, weight, over-banding, ease of assembly and manufacturablity
- **HTS assembly** – Tape per element, RUL per element, element energy capability, connectors, size, cooling orientation, failure mechanisms and mitigation, losses and their effects on cryogenics design
- **HV design** – LN2 and GN2 design stress criteria, spacing between tapes, elements and modules, stress shield dimensions, using solid barriers or not, bushings and assembly integration, assembly supporting structure (post insulators), overall assembly to cryostat spacing and integration
- **Cryogenics** - LN2 flow control, LN2 and GN2 interface, pressurizing, safety issues, thermal handling of fault and steady state losses
- **Sub-cooled Pressurized** – Improves the Recovery Under Load performance and enhances current carry capabilties.
- **Improvement of LN2 dielectric performance** – Pressurized LN2 helps to increase dielectric properties, avoiding bubbles and lowering breakdown voltage probability.

Sub-cooled Pressurized SFCL Device



Proof-of-concept demonstrated up to today

- Fault Current Testing with MCP 2212 (2004)
- Fault Current Testing with 2G YBCO (2006)
- Completed design and testing of HV bushings (ORNL, SEI, 2006)
- Weibull 2G failure study of ‘standard’ HTS superconductor architectures (2006)
- Investigated several engineered 2G architectures for improved RUL (2008)
- Improve connector design (2008)
- Modify 2G conductor to improve performance for FCL application (2008)
- Designed / tested compact 55kA shunt coils to withstand high fault transient loads (2008)
- Thermal simulation of RUL process (2008)
- Demonstrated Recovery Under Load (RUL) proof of concept and requirements (2008)
- Investigated LN2 dielectric properties (with ORNL, 2005-2008)
- Beta device testing specifications established (2008)
- Study of the Impact of bubbles on breakdown mechanism and LN_2 dielectric strength (with ORNL 2008)
- Improved understanding of the impacts of recovery under load (RUL) for module design (2009)
- Optimized performance of the 2G HTS wire (2009)
- Investigated the performance of more compact alternate ‘module’ concepts (2009)
- Tested FCL module components at rated voltage in a cryogenic environment (2009)
- Sub-cooled pressurized LN_2 environment testing (2010)
- Sub-cooled configuration of ‘engineered’ 2G conductor (2010)
- Sub-cooled LN_2 dielectric performance improvement (2010)

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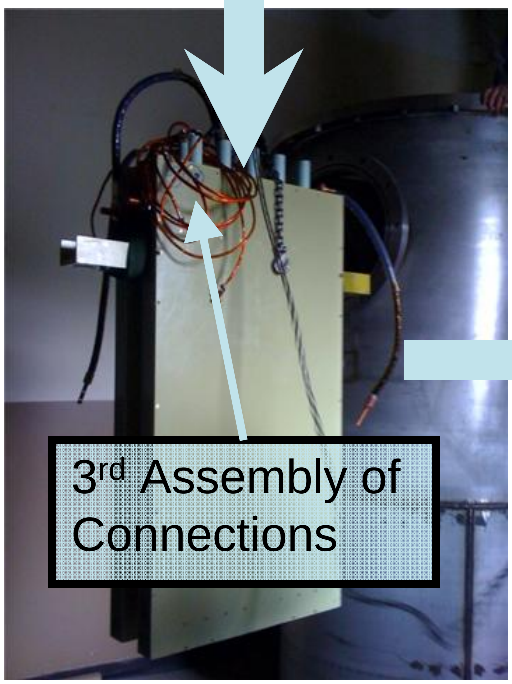
SFCL module manufacturing and assembly

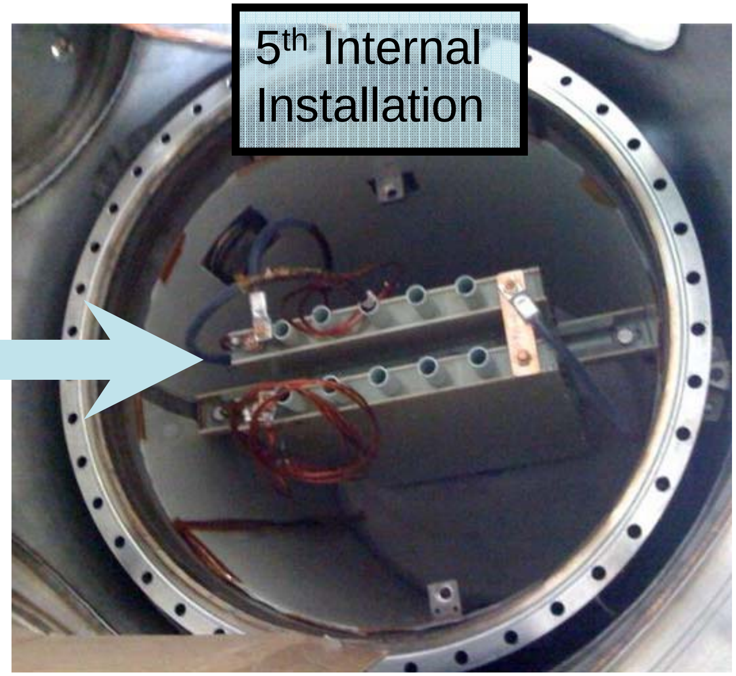
1st SFCL Module Manufacturing

2nd Assembly of Supports



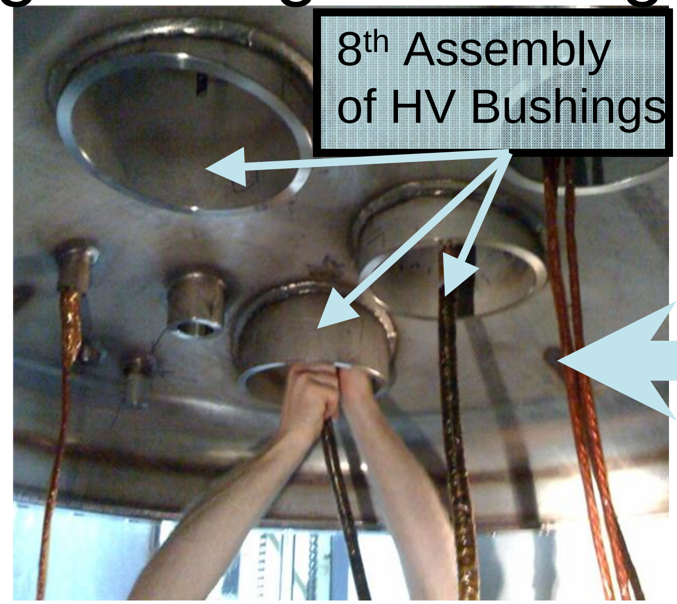
3rd Assembly of Connections

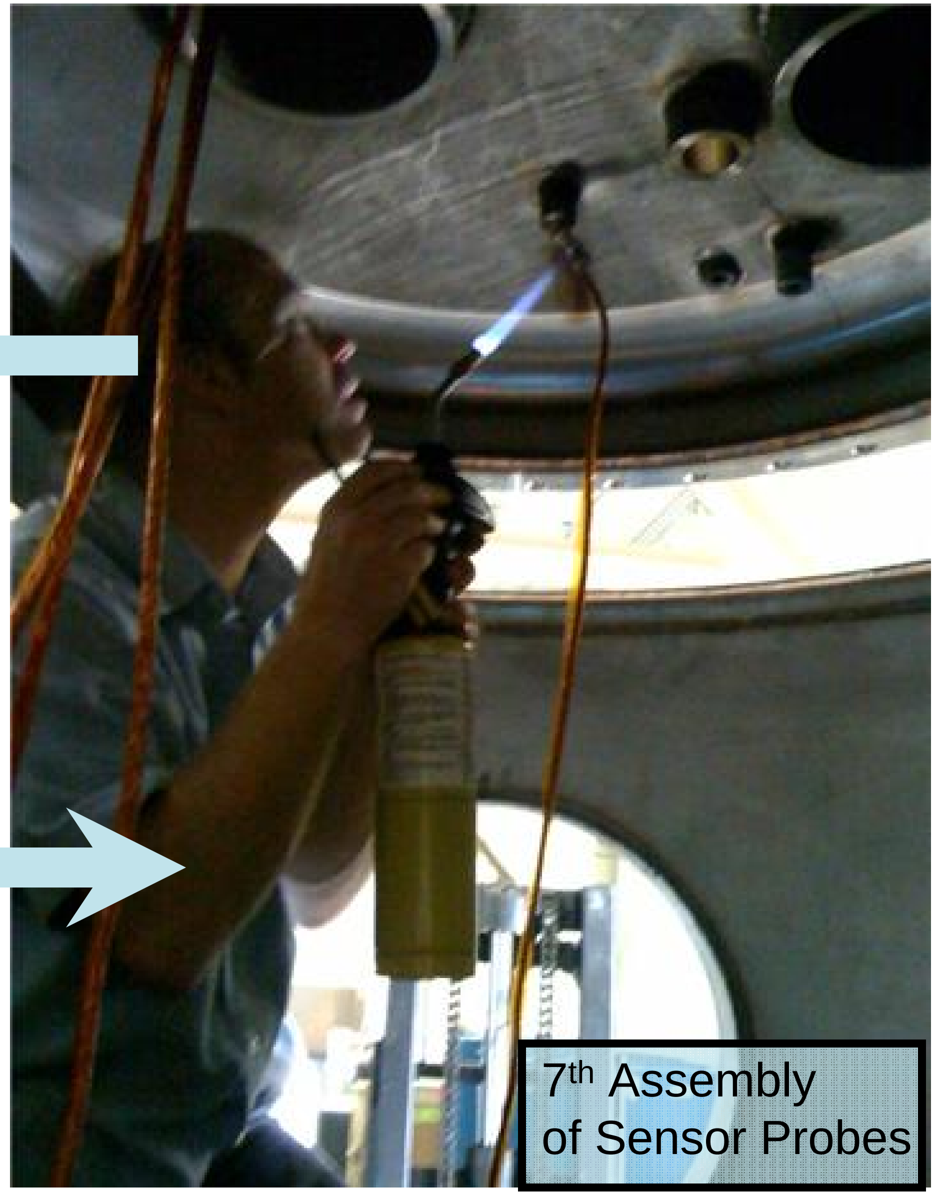
4th Module Installation



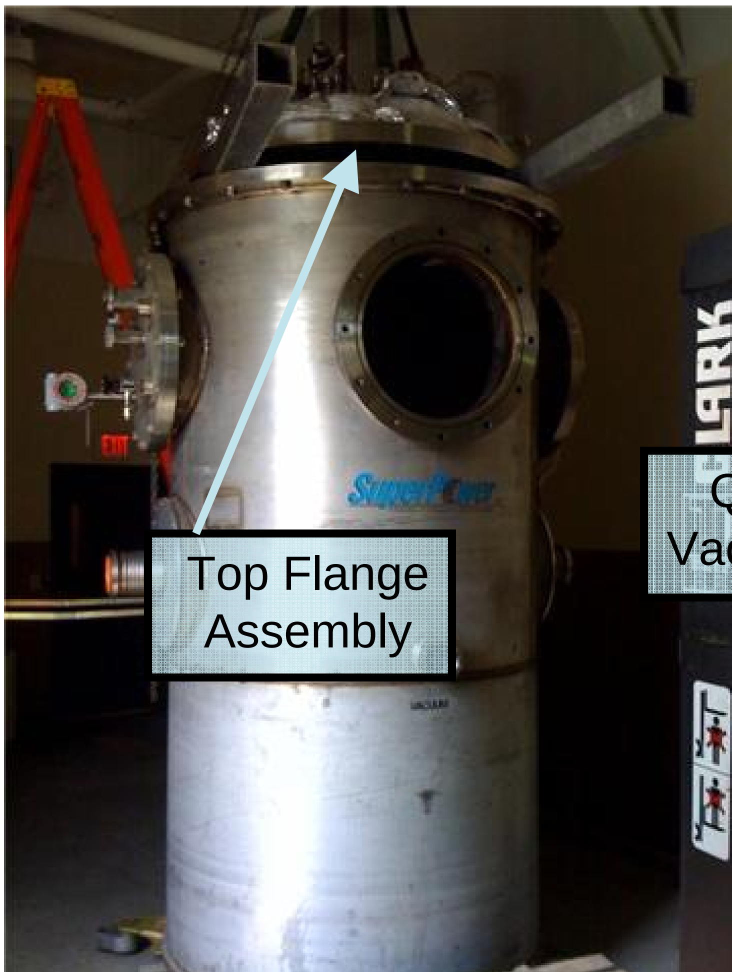
5th Internal Installation

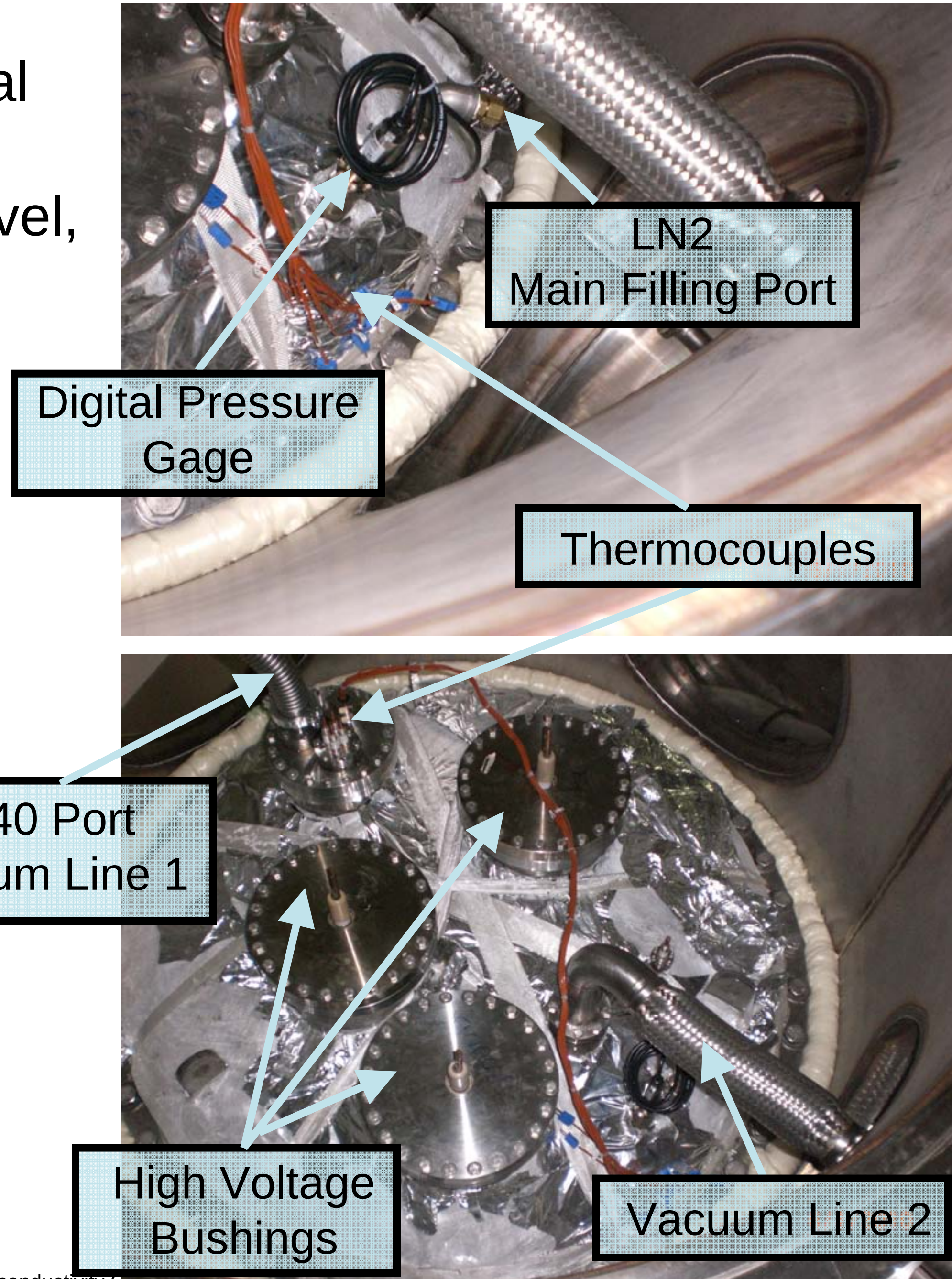
High voltage bushing and sensors installation





Pressure vacuum lines, digital pressure sensors, thermocouples, LN_2 ports, level, vent and relief valves





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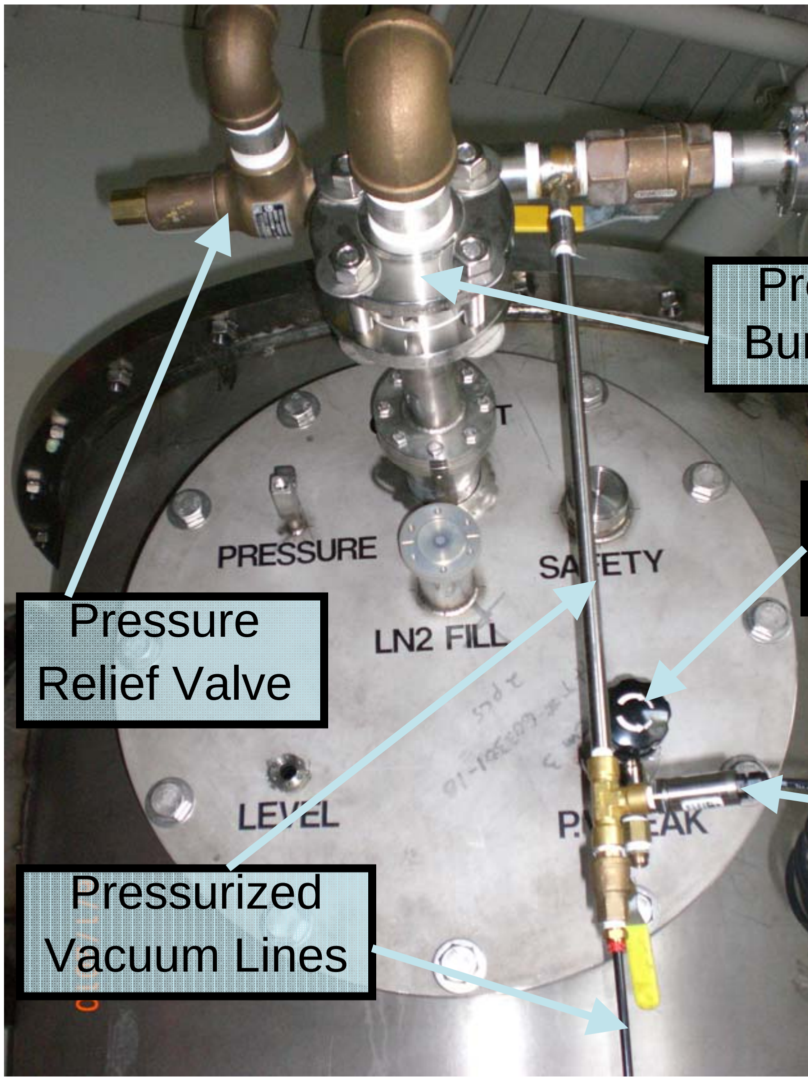
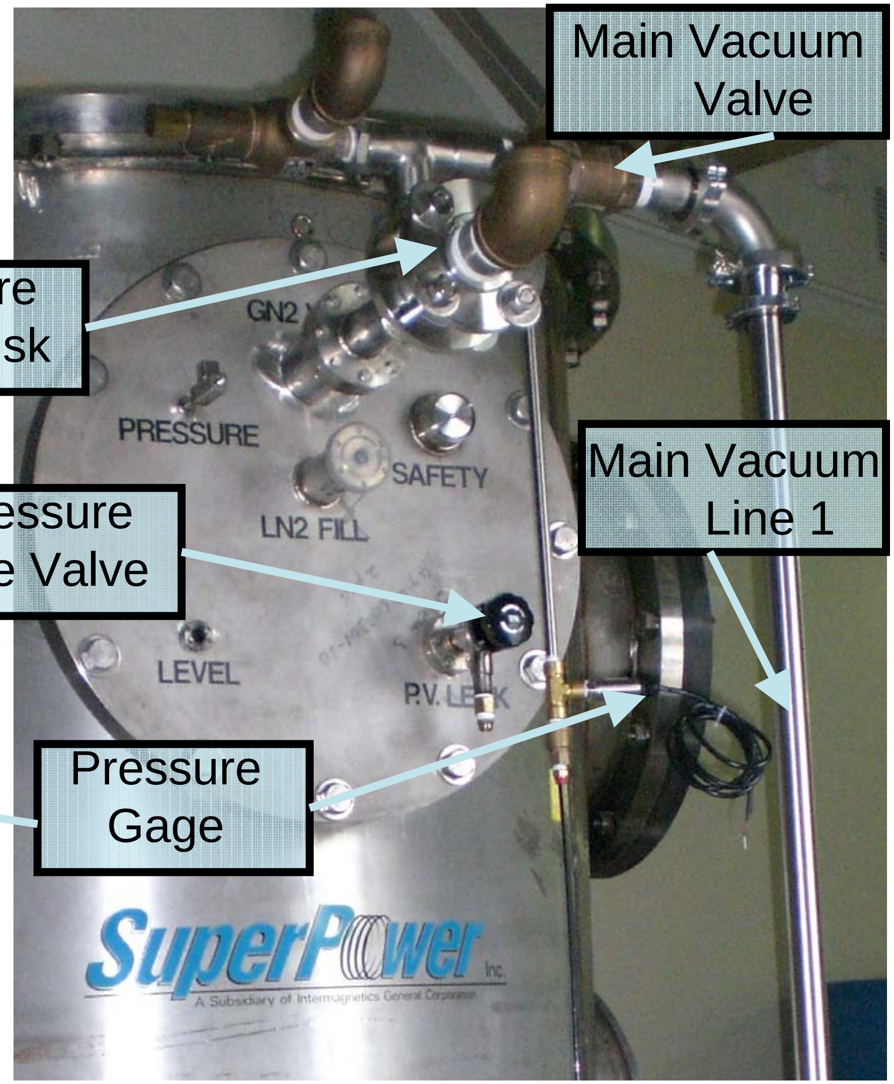
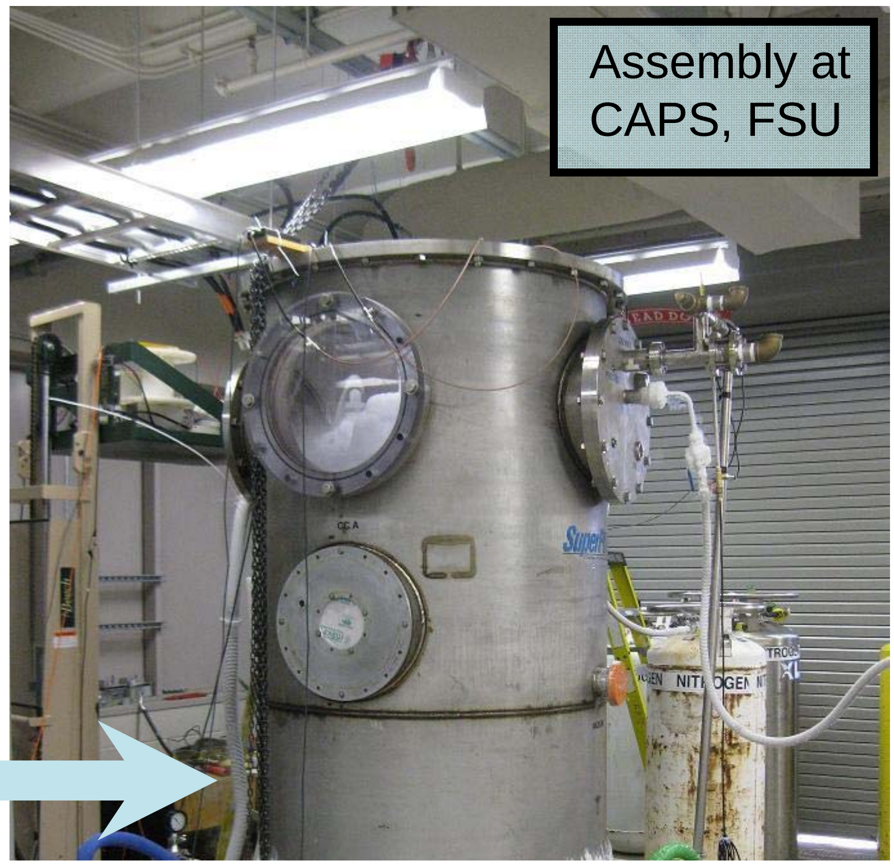




Shipping the SFCL to the Center for Advanced Power Systems (CAPS) at FSU in Tallahassee, FL



FSU-CAPS testing power in 2010

Real Time Simulator RTDS

4.16 kV utility bus

AC Voltage feedback to RTDS

AC current reference from RTDS

0… 4.16 kV / 5 MVA experimental bus

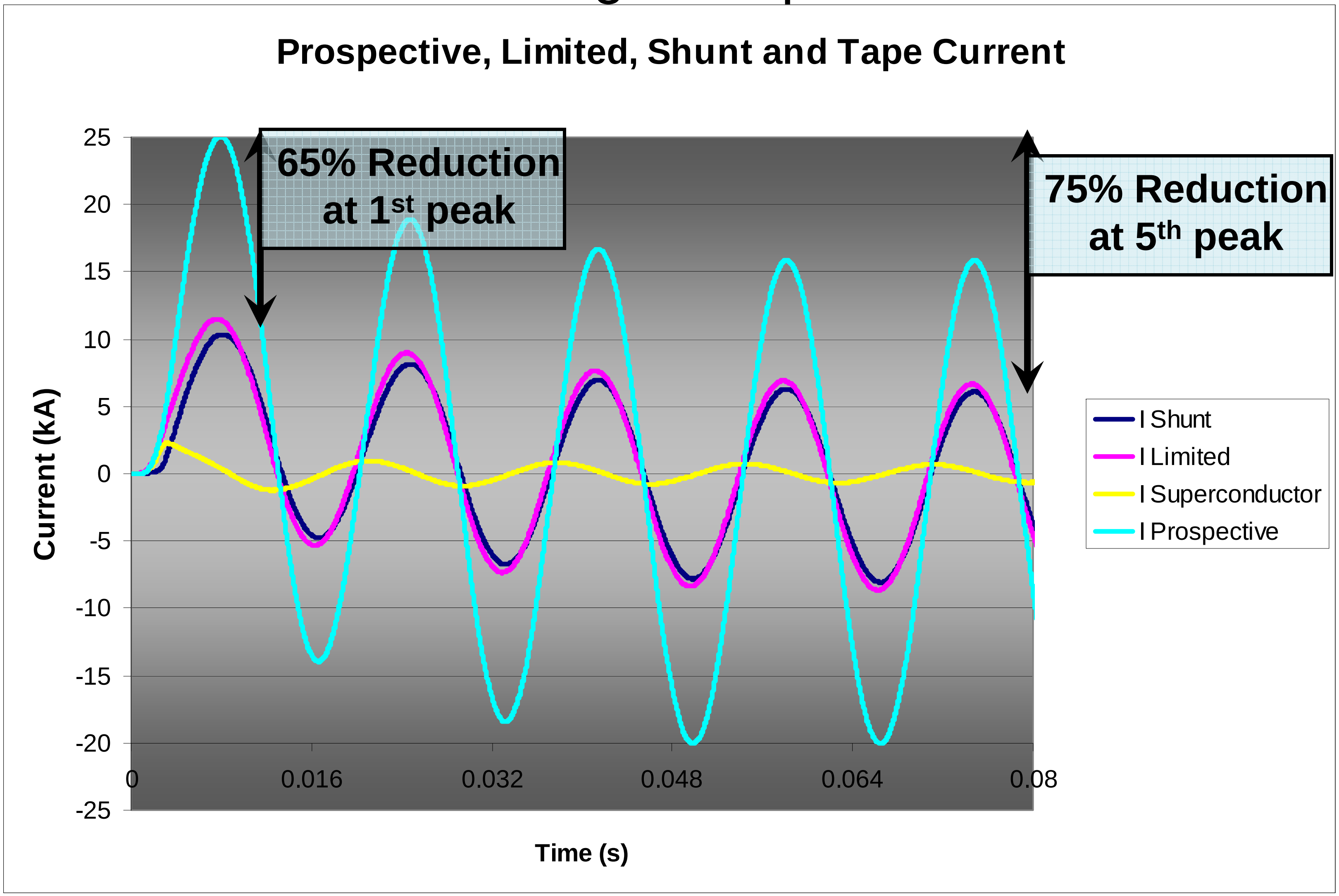
SFCL Device

5 MVA power available in **2010**

5 MW Converter "Amplifier"

SFCL Device under test

Limited current with a single 2 tape circuit in a module



65% Fault reduction at 1st peak with 2 tape circuit for a prospective of 26kA

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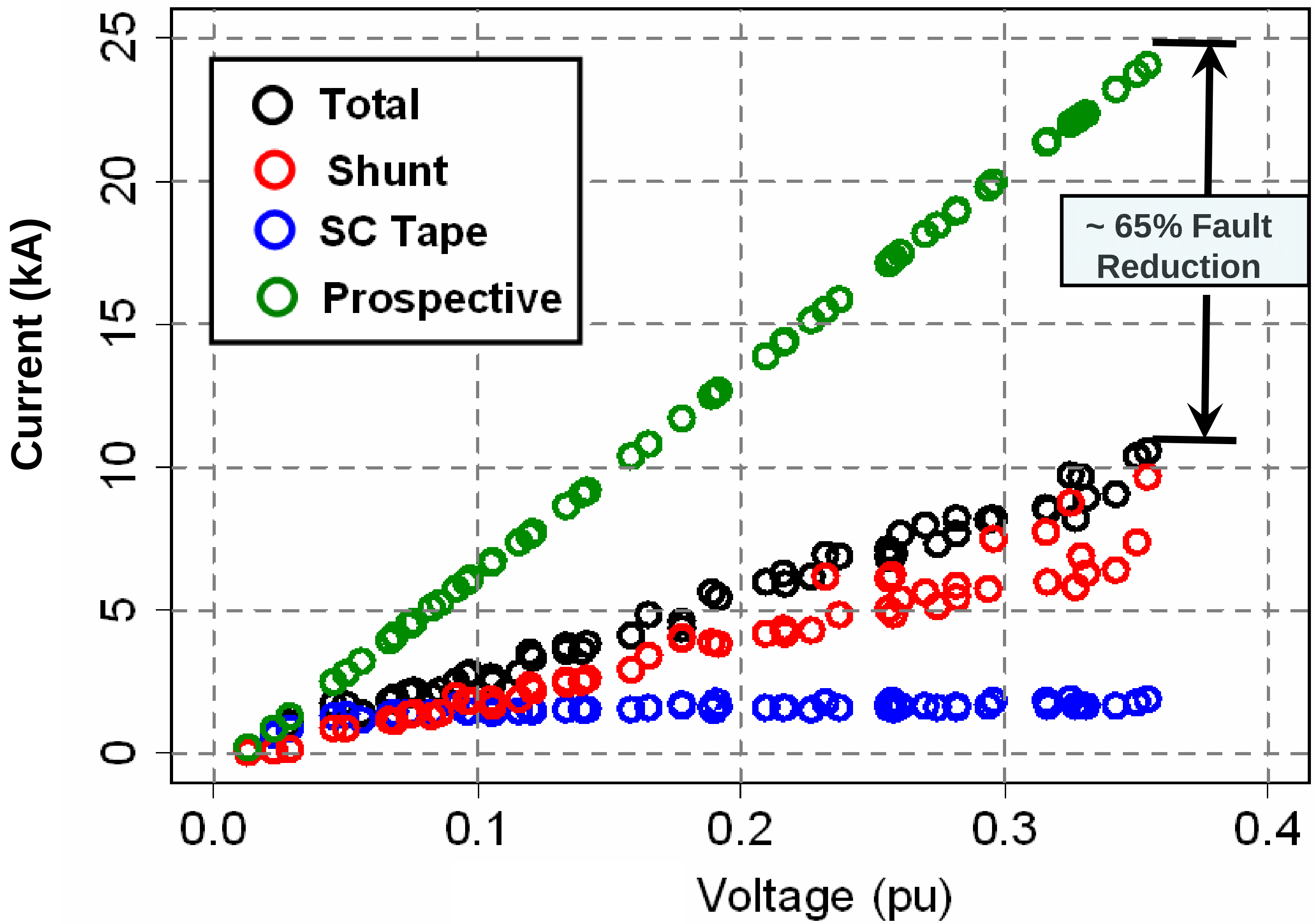
1st peak limited current for a 2 tape circuit vs. voltage



A single circuit of 2 tapes in a SFCL module will limit 65% of 1st peak fault in the entire voltage range (up to 25kA prospective tested at CAPS)

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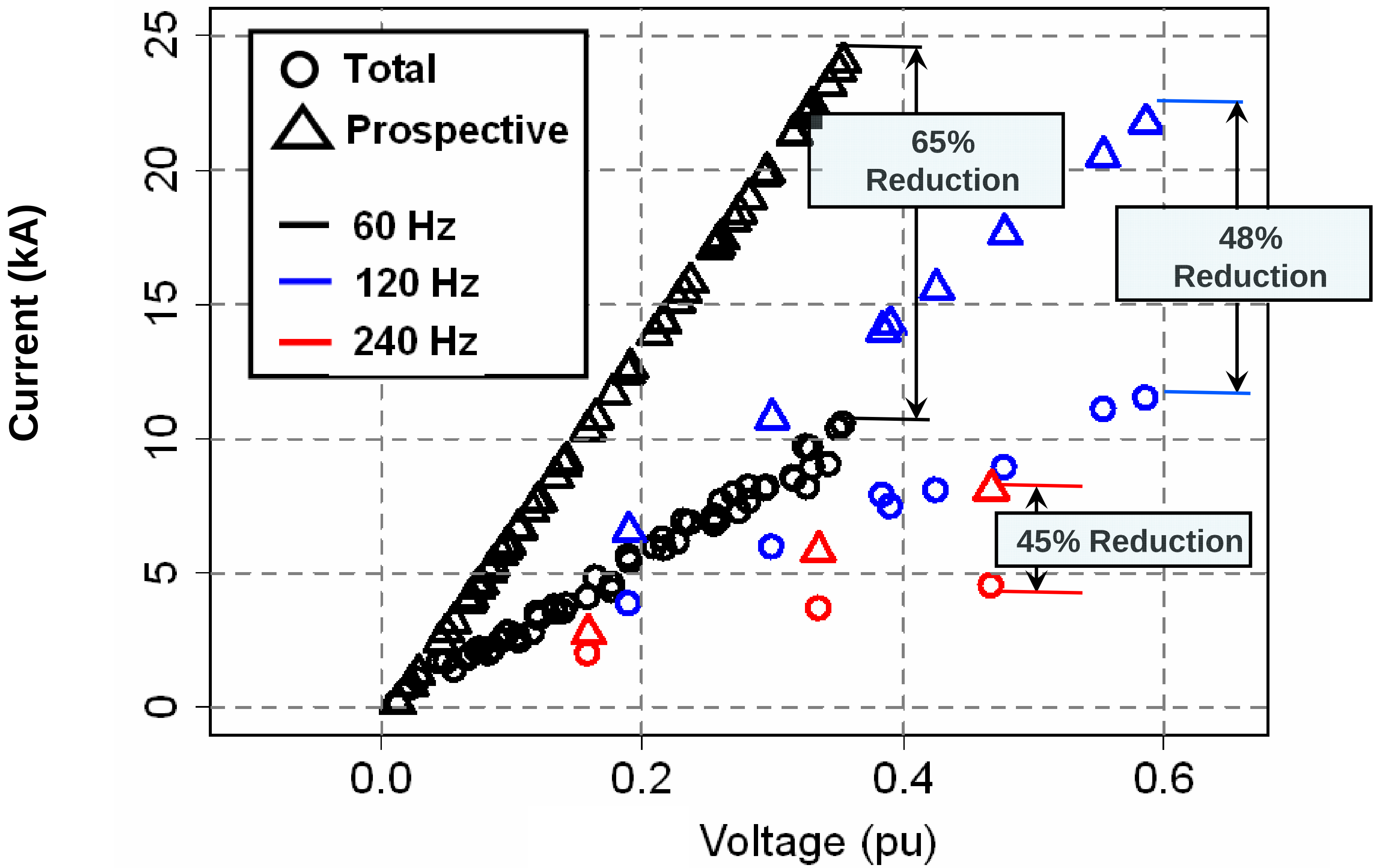
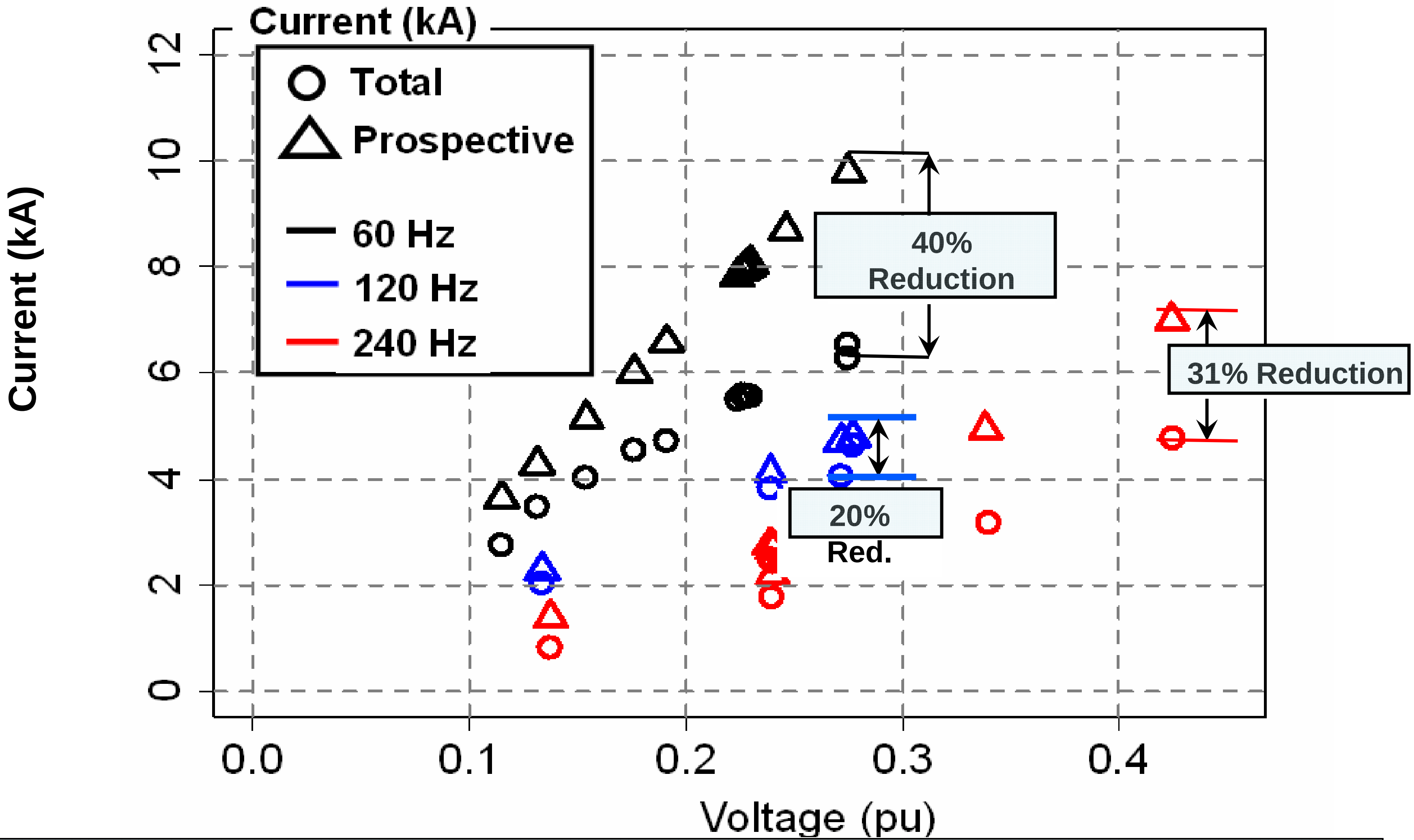
1st peak current for 2 tapes vs. voltage and frequency



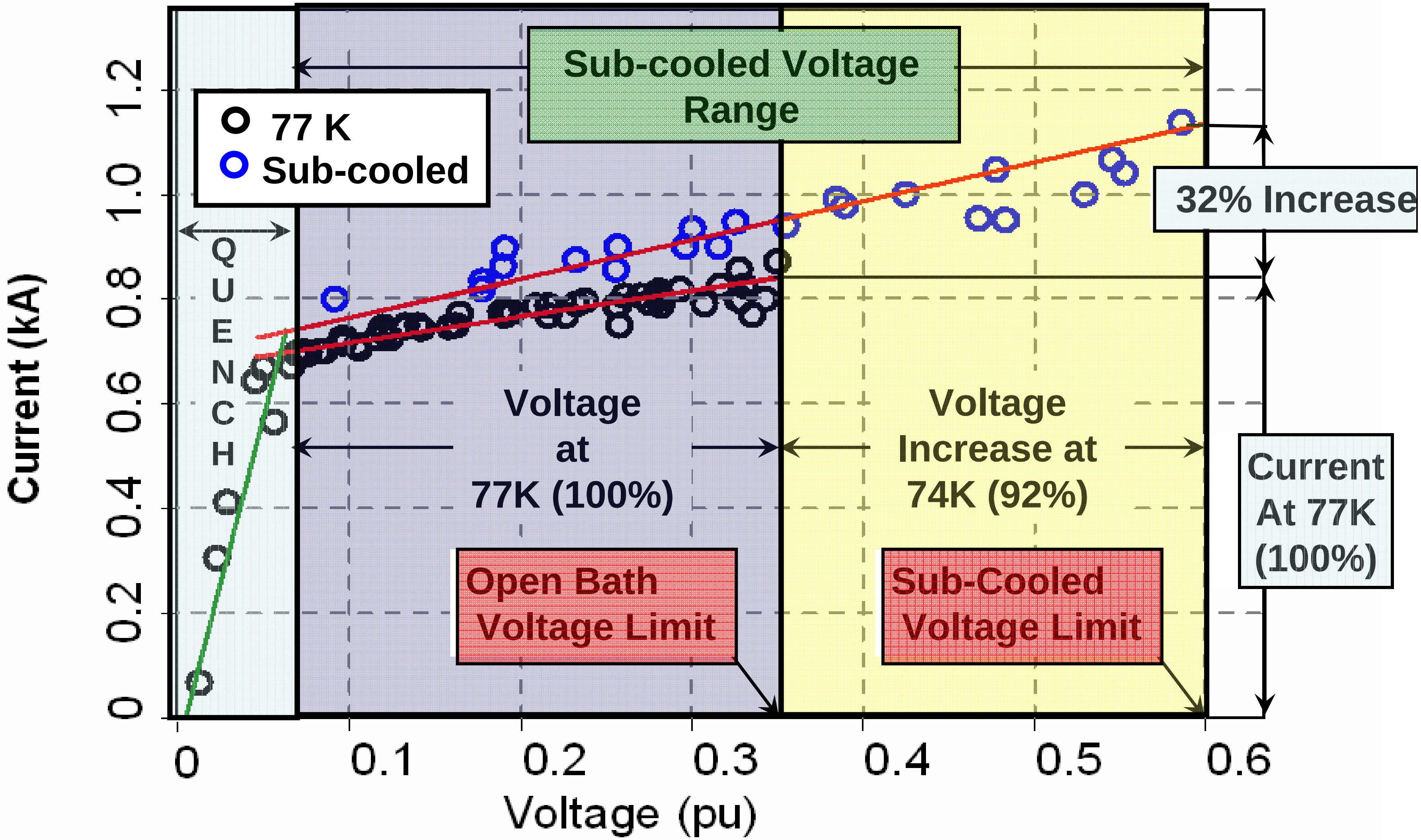
Current at different frequencies play a critical role in tape performance due to eddy current, skin depth on tape and non-homogeneous inductance at quenching.

1st peak current for 2 tapes vs. voltage and frequency



Different tape architecture also plays an important role in the overall system percentage fault limitation at different frequencies.

Peak load current per tape and voltage for 74K and 77K



Sub-cooled conditions at 74K improved 92% voltage (192% increase) and 32% more current (132%), a total of **~253% increase in power**.

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Generalized modular SFCL specification development in 2009 vs. 2010 up today

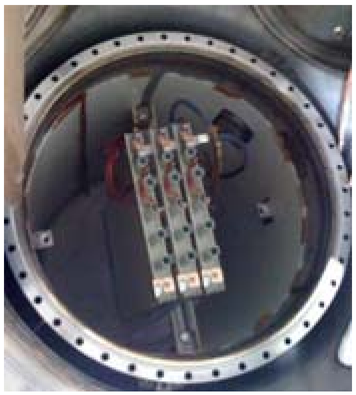
- 2009 Milestones of the modular baseline design for transmission and distribution lines
  - Module current scalable in multiples of **500 A** peak
  - Module voltage scalable from **400 V - 1 kV** peak
  - Prospective fault currents scalable from **5 - 10 kA** peak

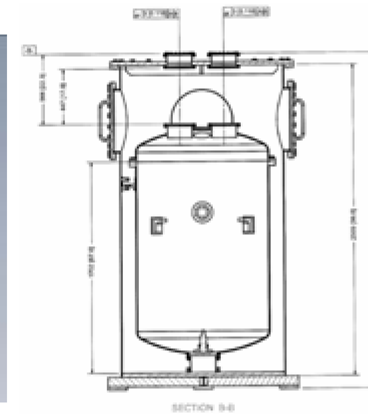
- 2010 testing for modular baseline design for transmission and distribution lines
  - Module load current capable of carrying **4kA** peak tested with sub-cooled LN_2 at **74K**
  - Module voltage tested with capability of driving **4kV** peak at 77K, and >**7KV** sub-cooled at **74K**.
  - Prospective modular fault current testing of **25 kA** peak at CAPS, previously tested up to **40kA** peak at **77K** at KEMA.
  - New sub-cooled SFCL modules are able to handle faults of **65kA** peak when sub-cooled at **74K.**

Generalized SFCL specification development

- The modular design permits scale-up of validated voltages and currents to accomplish Distribution and Transmission levels
- The number of modules used are based on the voltage / current requirements of the application

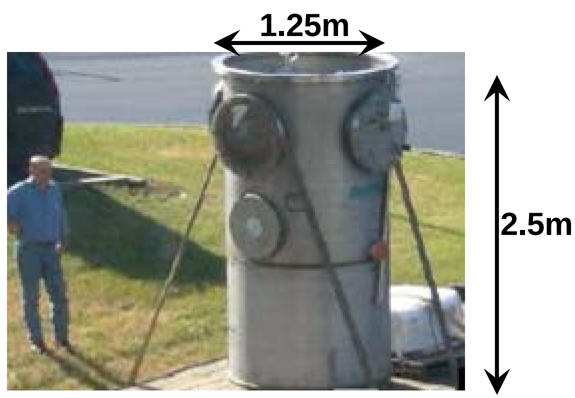
A **Distribution SCFL** 11-15kV phase, 800-2KA$_{rms}$ load current will limit ~65-75% when assembled with **3 SFCL modules**

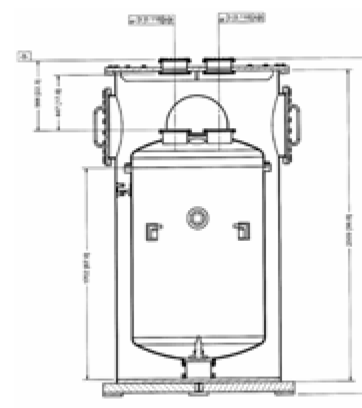




Distribution SCFL 15kV phase illustration

A **Transmission SCFL** 138kV phase, 1700A$_{rms}$ load, 40kA prospective will limit ~65-75% if assembled with **14 SFCL modules**





Transmission SCFL 138kV phase illustration

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Summary

- Focus on SFCL module development for distribution/transmission devices.
- Significant progress in:
  - Sub-cooled performance
    - Sub-cooled modular elements were developed and tested in 2010
    - Sub-cooled modular elements increase 132% current at 74K
    - Sub-cooled modular elements increase 192% voltage at 74K
    - Total Sub-cooled modular elements increase of 253% in power at 74K
    - Further testing study down to 65K range will be evaluated for the modular elements
  - $LN_{2\ d}$ielectrics
    - Further dielectric strength testing has been evaluated for the modular elements
  - Sub-cooled high voltage testing
    - Further sub-cooled High Voltage testing will be evaluated for the modular elements

Summary

- Frequency and Harmonics study
  - First study of frequency impact on 2G has been evaluated for 60Hz, 120Hz, and 240Hz.
  - Larger range of harmonic and current frequencies testing and study is underway.

- Overall system design reduction
  - In our SFCL design, any improvement in 2G architecture performance directly translates into a proportional reduction on the overall cryogenics and system cost.
  - Although there should be additional improvement in voltage at 65K that we are not accounting at this time, previous testing has shown an improvement in current around 200% at 65K from the present improvement of 253% at 74K.
  - The expected 200% improvement of just in the modular current at 65K together with the 253% power improvement achieved this year at 74K will yield a combined improvement in power of at least 506%.

Summary

- Present improvements in modules will permit to build:
  - A single Distribution SCFL phase of 11-15kV, 800-2KArms load, with ~65-70% limitation if assembled with 3 SFCL modules
  - A Transmission SCFL phase of 138kV, 1700Arms load, 40kA prospective limited between ~65-70% if assembled with 14 SFCL modules
- Great interest received from different customers to integrate our SFCL technology to develop SFCL devices and other kinds of superconducting devices built with SFCL capabilities

Questions?

Please contact:

jllambes@superpower-inc.com

www.superpower-inc.com